IN THE SPECIFICATION:

Please amend the specification as follows. A marked-up version of the amended paragraphs is provided as an attachment. A marked-up version of the amended title of the invention is not included.

On the cover page of the application, on page 1 of the specification and on page 30, Abstract of the Disclosure, please replace the title with:

-- SYSTEMS AND METHODS FOR EFFICIENT PROCESSING OF MULTIMEDIA DATA --

On page 6 of the specification, replace the paragraph beginning at line 15 with:

Media processor 32 may include several communication connections for communicating between media processor 32 and the rest of media processing system 30. A media_data connection 50 permits the transfer of media data between media processor 32 and other systems, such as compressed image generator 25 (Figure 1). A media_control connection 52 transfers control signals and/or data between media processor 32 and other systems, such as intelligent interface controller (I^2C) compatible devices and/or interface hardware connected to system bus 41. A user_interface connection 54 transfers user interface data between media processor 32 and user interface peripherals, such as joysticks, IR remote control devices, etc. Finally, an input/output channel connection 56 allows for connections to other I/O devices for further expansion of the system.

a1

On page 8 of the specification, replace the paragraph beginning at line 9 with:

In one embodiment, communication bus 60 is another 32-bit bus, with a maximum data transfer rate of around 172 Mbytes/sec, and is used for transferring 128-bit packets either between the MPEs, or to allow MPEs to talk to peripheral devices. Communication bus 60 is a low latency bus, and is good for inter-processor communications. For a more detailed discussion of communication bus 60, see U.S. Patent Application No. 09/476,946, filed January 3, 2000, and entitled "Communication Bus for a Multi-processor System," the entirety of which is incorporated herein by reference.

a2

On page 11 of the specification, replace the paragraph beginning at line 5 with:

After all the audio, video and DVD information is decoded and placed in memory, display generator 80 retrieves the video, subpicture and control information from memory and performs some processing. For example, in accordance with one embodiment of the present invention, the video information is stored in memory in 4:2:0 MPEG format. Display generator 80 converts the 4:2:0 format to 4:2:2 format, which is consistent with CCIR 656 standard video format. In addition, display generator 80 combines video information with overlay information, such as menus and the like, and subpicture channel information and presents the entire packet of information as an output. Finally, display generator 80 is configured to perform video timing and refresh functions, and may perform some of the subpicture decoding operations. A more detailed description of how display generator 80 interacts with one or more of the MPEs to perform subpicture decode is set forth in U.S. Patent Application No. 09/476,698, filed January 3, 2000, and entitled "Subpicture Decoding Methods and Apparatus," the entirety of which is incorporated herein by reference.

a3

On page 14 of the specification, replace the paragraph beginning a line 4 with:

Architecture 100 of the MPEs may have a plurality of sub-units, such as an execution control unit (ECU) 106, a memory processing unit (MEM) 108, a register control unit (RCU) 110, an arithmetic logic unit (ALU) 112, a multiplication processing unit (MUL) 114, and a register file 116. In one embodiment, ECM 106, MEM 108, RCU 110, ALU 112 and MUL 114 all are connected together in parallel via register file 116. An Instruction Decompression and Routing unit 118 is connected to an instruction memory 120 via instruction bus 102, and is configured to decode and route instructions to the various processing units within the MPE. Instruction memory 120 stores a plurality of instructions, which control the various processing units in the MPE. The stored instructions are in the form of very long instruction word (VLIW) instructions, which, in one embodiment, have been compressed to reduce the amount of memory required to store the instructions. A more detailed discussion of the VLIW compression is set forth below.

a4

On pages 22 and 23 of the specification, replace the paragraph beginning at line 29 of page 22 with:

ALU 112 includes a plurality of switches 210, 212, and 214, such as multiplexers or the like, which are configured to select data from one of a number of source inputs of ALU 112. For example, switch 210 may select data from a Src A, which in accordance with the present invention is a 32-bit data type stored in any one of the registers, or from immediate data (ImmB) stored in the ALU instructions. Similarly, second switch 212 may select data from Src A, or from an immediate value (ImmA) stored in the ALU instruction. The ImmA immediate data also may be sign extended by a sign extender 216 prior to entering the switch. The ImmA data, Src B data, Src D data, or the most significant bits of Src B data may be selected by third switch 214. The most significant bits of Src B data may be determined by a most significant bit (MSB) unit 217.

a5